CLAIM LISTING

This listing of claims will replace all prior versions, and listings of claims in the application:

AMENDMENTS TO THE CLAIMS

1.-14. (Cancelled)

15. (Currently Amended) A distributed buffering system comprises:

input buffer that includes a plurality of input memories, wherein the input buffer stores at least one data block and wherein each of the plurality of input memories stores a corresponding portion of the at least one data block;

plurality of serializing modules operably coupled to the plurality of input memories, wherein each of the plurality of serializing modules serializes the corresponding portion of the at least one data block to produce a plurality of streams of data;

programmable logic device operably coupled to distribute the plurality of streams of data to at least one of a plurality of output buffers based on a distribute instruction, wherein each of the plurality of output buffers includes a plurality of output memories;[[and]]

plurality of deserializing modules, wherein each of the plurality of deserializing modules is operably coupled to a corresponding one of the plurality of output memories of each of the plurality of output buffers, wherein corresponding ones of the plurality of deserializing modules deserializes a corresponding one of the plurality of streams of data to recapture the corresponding portions of the at least one block of data, wherein the plurality of output memories of the at least one of the output buffers stores the recaptured corresponding portions of the at least one block data; and

controller operably coupled to the input buffer, the programmable logic, and the plurality of output buffers, wherein the controller generates the distribute instruction, generates a plurality of read instructions, and a plurality of write instructions, wherein the plurality of read instructions are provided to the plurality of input memories, and wherein the plurality of write instructions are provided to the plurality of output memories of the at least one of the plurality of output buffers.

16. (Cancelled)

17. (Currently Amended) The distributed buffering system of claim[[16]] 15, wherein the controller further comprises:

aligning module operably coupled to align access to the recaptured corresponding portions of the at least one data block from the plurality of output memories of the at least one of the plurality of output buffers.

18. (Original) The distributed buffering system of claim 17, wherein the controller further comprises:

propagation module operably coupled to maintain propagation delay information for each path between the programmable logic device and the plurality of input memories and for each path between the programmable logic device and the plurality of output memories of the each of the plurality of output buffers.

19. (Original) The distributed buffering system of claim 18, wherein the controller further comprises:

training module operably coupled to provide test data over each of the paths between the programmable logic device and the plurality of input memories and over each of the paths between the programmable logic device and the plurality of output memories of the each of the plurality of output buffers, wherein the propagation module determines the propagation delay information based on the test data.

20. (Original) The distributed buffering system of claim 18, wherein the programmable logic device further comprises:

memory operably coupled to provide buffering for at least some of the paths between the programmable logic device and the plurality of input memories and the paths between the programmable logic device and the plurality of output memories of the each of the plurality of output buffers to facilitate the align access to the recaptured corresponding portions of the at least one data block.

21. (Currently Amended) The distributed buffering system of claim[[16]] 15, wherein the controller further comprises:

instruction buffer operably coupled to queue incoming instructions based on propagation delay of distributing the at least one data block between the input buffer and the at least one of the plurality output buffers.

22. (Currently Amended) The distributed buffering system of claim[[16]] 15, wherein the controller further comprises:

synchronizing module operably coupled to synchronize distributing the at least one data block between the input buffer and the at least one of the plurality of output buffers.

23.-69. (Cancelled)

70. (New) The distributed buffering system of claim 15, wherein the controller is implemented as a memory control module operably coupled to the input buffer, the programmable logic device, and the at least one output buffer, wherein the memory control module generates a read instruction and generates a write instruction based on the distribution instruction, wherein the read instruction is provided to the input buffer and the write instruction is provided to the at least one output buffer.

71. (New) The distributed buffering system of claim 70 further comprises:

a programmable gate array programmed to function as the memory control module and to function as the programmable logic device for distributing the serial stream of data.

72. (New) The distributed buffering system of claim 15 further comprises:

an input integrated circuit that includes the input buffer and the serializing module; and

a plurality of output integrated circuits, wherein each of the plurality of output integrated circuits includes an output buffer and a corresponding deserializing module.

73. (New) The distributed buffering system of claim 15, wherein the at least one output buffer includes a plurality of output buffers, wherein the at least one deserializing module includes a plurality of deserializing modules, and wherein the programmable logic device further comprises:

input interface operably coupled to receive the serial stream of data;

plurality of output interfaces operably coupled to the plurality of output buffers; and

programmable logic fabric operable to provide selective connectivity between the input interface and the plurality of output interfaces, wherein the input interface deserializes the serial stream of data to produce deserialized data and wherein each of the plurality of output interfaces selectively connected to the input interface serializes the deserialized data to recapture the serial stream of data.

74. (New) The distributed buffering system of claim 15 further comprises:

a plurality of input buffers that include the input buffer; and

a plurality of serializing modules that include the serializing module, wherein the plurality of serializing modules is operably coupled to the plurality of input buffers.

75. (New) The distributed buffering system of claim 15, wherein the serializing module further comprises a rate adjusting module that establishes bit rate of the serializing module based on rate of the input buffer and data width of the input buffer.

76. (New) The distributing buffering system of claim 75, wherein the at least one output buffers further comprise a rate adjusting module that establishes bit rate of the at least one output buffer based on the rate of the input buffer and the data width of the input buffer.

77. (New) The distributed buffering system of claim 75, wherein the at least one output buffer further comprise rate adjusting module that establishes bit rate of the at least one output buffer based on rate of the at least one output buffer and data width of the at least one output buffer.

78. (New) The distributed buffering system of claim 15, wherein the programmable logic device further comprises a command module operably coupled to receive a buffering instruction, wherein the command module generates the distribution instruction and a logic configuration signal based on the buffering instruction, wherein the logic configuration signal configures logic of the programmable logic device.

79. (New) The distributed buffering system of claim 15, wherein the programmable logic device further comprises a clock module operably coupled to generate clocking signals, wherein the clock module provides the clocking signals to the input buffer, the serializing module, the plurality of deserializing modules, and the plurality of output buffers.

80. (New) The distributed buffering system of claim 15, wherein the serializing module further comprises an addressing module operably coupled to serialize, as part of the serial stream of data, at least one address of the at least one of the plurality of output buffers based on a buffering instruction, and wherein the programmable logic device includes an interpreting module to extract the at least one address from the serial stream of data.

81. (New) The distributed buffering system of claim 15, wherein the programmable logic device further comprises memory operably coupled to buffer the serial stream of data, to delay providing of the serial stream of data to the at least one output buffer, or to cache the serial stream of data for the at least one output buffer.

82. (New) The distributed buffering system of claim 15, wherein the input buffer further comprises a plurality of memories operably coupled to the serializing module, wherein each of the plurality of memories stores a corresponding portion of the at least one data block.